Claims 1-3, 7-8 and 22-23 were rejected under 35 U.S.C. 102(b) as unpatentable over U.S. Patent No. 6,002,147 to Iovdalsky et al. (hereinafter "Iovdalsky"). The rejection is respectfully traversed.

First, the Examiner stated at page 2 of the office action that "It should be noted that the device 1 is considered as a semiconductor chip or substrate." However, it appears that the device 1 in Iovdalsky is described in the patent as a "dielectric board". See Iovdalsky at col. 2, line 66. Applicant respectfully submits that the Examiner cited no portion of the art that establishes that the "dielectric board" of Iovdalsky is a "semiconductor chip" as recited in claim 1. Accordingly, applicant respectfully submits that the Examiner has cited no portion of Iovdalsky that describes a "digging a hole from a second surface of the semiconductor chip" as recited in claim 1. Accordingly, applicant respectfully requests that the rejection of claim 1 and its dependent claims 2-3 and 7-8 be withdrawn.

Claim 22 has been canceled without prejudice. Claim 23 has been rewritten in independent form. The Examiner stated at page 3 of the office action that in Lovdalsky, "the layer 11 is considered as an electric layer since it prevents a short circuit between the substrates." Applicant respectfully disagrees with the Examiner's statement. An electric layer would not prevent a short circuit between substrates. Indeed, the layer 11 of Iovdalsky "an electrically and heat conducting material 11, e.g., an (Au-Si) solder." Iovdalsky at col. 3, lines 24-25. Thus, the layer 11 does not appear to be a dielectric material. Accordingly, applicant respectfully submits that the Examiner cited no potion of the art that describes or suggests "forming a dielectric layer on at least one of the first substrate and second substrate and positioning the dielectric layer to prevent a short circuit between the first substrate and second substrate" as recited in claim 23.

Claims 4-6 were rejected under 35 U.S.C. 103(a) as unpatentable over Iovdalsky in view of U.S. Patent No. 6,453,893 to Khandros et al. ("Khandros"). The rejection is respectfully traversed. Applicant respectfully submits that Iovdalsky is deficient for at least similar reasons as discussed for claim 1 above. In addition, applicant respectfully submits that the Examiner cited no portion of Khandros that overcome the deficiencies of Lovdalsky. In addition, with respect to claim 6, applicant respectfully submits that the Examiner cited no portion of the art that describes or suggests "forming a hole by an anodic forming method using a dielectric layer coated on an opposite surface of the first semiconductor chip as a mask, thereafter removing the metal film,

and forming an electrode on a portion of the surface of the first semiconductor chip in a manner to embed the hole" as recited in claim 6. Accordingly, for at least the above reasons, applicant requests that the rejection of claims 4-6 be withdrawn.

New claims 24-37 have been added. Support for these claims may be found throughout the specification, figures and original claims. It is believed that no new subject matter has been entered. Examination of the new claims is respectfully requested.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-8 and 23-37 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes

Alan S. Raynes
Reg. No. 39,809
KONRAD RAYNES VICTOR & MANN, LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212
Customer No. 24033

Dated: March 31, 2003

(310) 556-7983 (tele general)
(310) 871-8448 (tele direct)
(310) 556-7984 (facsimile)

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Alan S. Raynes — March 31 , 2003

Alan S. Raynes **(Date)**

Version With Markings to Show Changes Made

Claims 4-5, 7-8 and 23 were amended as follows:

4. (amended) A method for manufacturing a semiconductor chip, the method comprising: forming an electrode on a surface of a first semiconductor chip and thereafter forming a hole from another surface of the first semiconductor chip until the electrode is exposed, forming a protrusion by etching a surface of a second semiconductor chip and thereafter forming an abutting electrode on an apex section of the protrusion, and positioning the first semiconductor chip and the second semiconductor chip such that the abutting electrode is in electrical contact with [contacts] the electrode.

5. (amended) A method as in claim 4, wherein forming a hole from another surface comprises forming the [hold] hole from a surface that is opposite to the surface the electrode was formed on.

7. (amended) A method for manufacturing a semiconductor device according to claim 2, wherein, after the hole is formed, a metal film is formed on the electrode through the hole [from the opposite surface].

8. (amended) A method for manufacturing a semiconductor device according to claim 3, wherein, after the hole is formed, a metal film is formed on the first layer of the electrode so that the first layer of the electrode is positioned between the metal film and the second layer of the electrode [from the opposite surface].

23. (amended) A method for forming a semiconductor device [as in claim 22, further] comprising:

forming a first electrode on a first surface of a first substrate;

forming an opening from a second surface of the first substrate to the first surface, wherein a portion of the first electrode is exposed through the opening;

forming a second electrode on a second substrate;

forming a dielectric layer on at least one of the first substrate and second substrate and positioning the dielectric layer to prevent a short circuit between the first substrate and second substrate; and

positioning the second electrode in the opening and electrically connecting the first electrode to the second electrode.